

A Simple Four-Port Parasitic Deembedding Methodology for High-Frequency Scattering Parameter and Noise Characterization of SiGe HBTs

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Abstract—A new four-port scattering parameter (S -parameter) and broad-band noise deembedding methodology is presented. This deembedding technique considers distributed on-wafer parasitics in the millimeter-wave band ($f > 30$ GHz). The procedure is based on simple analytical calculations and requires no equivalent circuit modeling or electromagnetic simulations. Detailed four-port system analysis and deembedding expressions are derived. Comparisons between this new method and the industry-standard “open-short” method were made using measured and simulated data on state-of-the-art SiGe HBTs with a maximum cutoff frequency of approximately 180 GHz. The comparison demonstrates that better accuracy is achieved using this new four-port method. Based on a combination of measurements and HP-ADS simulations, we also show that this new technique can be used to accurately extract the S -parameters and broad-band noise characteristics to frequencies above 100 GHz.

Index Terms—Deembedding, noise, noise correlation matrix, parasitics, S -parameters, SiGe HBT, Y -parameters.

I. INTRODUCTION

THE accuracy of high-frequency characterization of state-of-the-art SiGe HBTs is important in both device modeling and circuit design. For accurate evaluation of the high-frequency characteristics, extraction of the transistor S -parameters and broad-band noise characteristics at very high frequencies is typically required. As the operating frequency increases into the microwave range, the on-wafer parasitic effects can become significant in such measurements, requiring robust calibration techniques in order to accurately deembed the parasitics from the transistor response.

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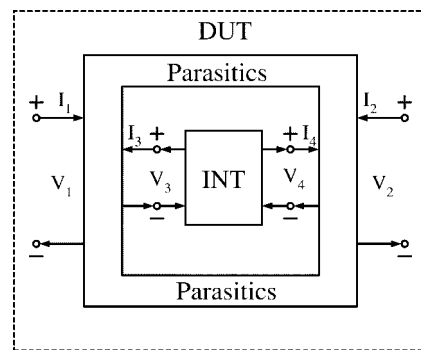


Fig. 1. Illustration of a general four-port structure. The two extrinsic ports of the DUT are denoted ports 1 and 2, and the two ports of intrinsic device (INT) are denoted ports 3 and 4.

The standard “open” deembedding method was first proposed in 1987 [1] and employs a technique in which the pad capacitance is accounted for and calibrated by using an “OPEN” test structure (i.e., no transistor). Several other deembedding methods were subsequently proposed, and which use additional test structures (including the “SHORT” and “THROUGH,” etc.) to calibrate both the pad and interconnect parasitics in the device-under-test (DUT) [2], [3].

The current industry paradigm is the so-called “open-short” standard [3]. However, since this approach assumes lumped-component approximations, it begins to lose accuracy as the frequency increases above approximately 30 GHz. For more robust S -parameter extraction, several high-frequency deembedding techniques have been recently proposed [6], [7]. These methods either use equivalent two-port analysis (with cascade, series, or parallel structures) or complicated equivalent circuit models, which simplify the parasitics under suitable approximations (e.g., the cascade structure neglects the parasitic feedback from the output to input).

To generalize the problem and avoid the potential inaccuracy caused by the above assumptions or simplifications, a four-port system calibration methodology was introduced by Rizzoli *et al.* for noise analysis [8]. As shown in [8] and [9], any two-port measurement can be modeled as a four-port system, which captures all of the parasitics surrounding the intrinsic device (Fig. 1). Once the 4×4 matrix of the system is solved, the intrinsic S -parameters can be accurately extracted. However,

the 4×4 matrix was solved either using equivalent-circuit [8], [9] or electrical magnetic (EM) simulations, together with additional calibration [10]. Clearly, the accuracy of such methods depends on the validity of the lumped or distributive model.

In this paper, we present a set of test structures that efficiently determine the Y -parameters of the four-port parasitic network *without requiring* any equivalent-circuit assumptions or EM simulations. Thus, this deembedding methodology considers all parasitics in a general manner, making it suitable for very high-frequency measurements and package parasitic decoupling. We apply this deembedding methodology to the characterization of state-of-the-art SiGe HBTs.

II. FOUR-PORT PARASITIC DEEMBEDDING THEORY

A. S -Parameters

As shown in Fig. 1, the parasitics are modeled as a four-port system. The I - V relationships of the extrinsic and intrinsic ports can be written as a 4×4 Y -matrix according to

$$\begin{pmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{pmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{pmatrix}. \quad (1)$$

In some circumstances, Y_{ij} can be ∞ (i.e., there is a short between various ports). In this case, let Y_{ij} be very large to avoid any singularities.

Let V_e and I_e be the extrinsic voltage and current vectors, and V_i and I_i be the intrinsic voltage and current vectors [10]

$$\begin{pmatrix} V_e \\ V_i \end{pmatrix} = \begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{pmatrix} \quad \text{and} \quad \begin{pmatrix} I_e \\ I_i \end{pmatrix} = \begin{pmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{pmatrix}.$$

Thus, we have [8]

$$\begin{pmatrix} I_e \\ I_i \end{pmatrix} = \begin{bmatrix} Y_{ee} & Y_{ei} \\ Y_{ie} & Y_{ii} \end{bmatrix} \begin{pmatrix} V_e \\ V_i \end{pmatrix} \quad (2)$$

where $[Y_{ee}]$, $[Y_{ei}]$, $[Y_{ie}]$, and $[Y_{ii}]$ are four 2×2 matrices. Hence, the extrinsic Y -parameters and the intrinsic device Y -parameters can then be related as

$$\begin{aligned} Y^{\text{DUT}} V_e &= Y_{ee} V_e + Y_{ei} V_i \\ -Y^{\text{INT}} V_i &= Y_{ie} V_e + Y_{ii} V_i \end{aligned}$$

where Y^{INT} are the intrinsic device Y -parameters and Y^{DUT} are the two-port Y -parameters of the DUT.

Note that the current directions of the intrinsic device are opposite to the current directions of the parasitics. One thus obtains

$$Y^{\text{DUT}} = Y_{ee} - Y_{ei}(Y^{\text{INT}} + Y_{ii})^{-1}Y_{ie} \quad (3)$$

or

$$Y^{\text{INT}} = -Y_{ie}(Y^{\text{DUT}} - Y_{ee})^{-1}Y_{ei} - Y_{ii}. \quad (4)$$

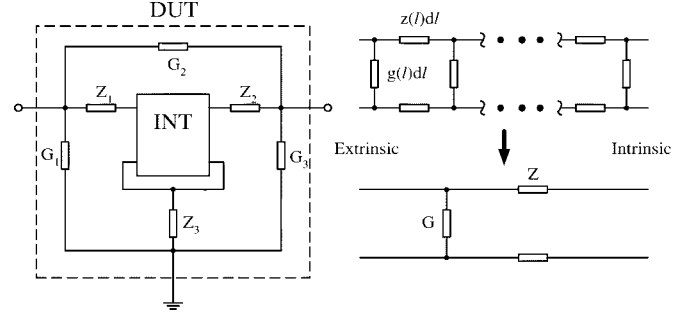


Fig. 2. Equivalent-circuit model of the traditional “open-short” deembedding method.

Once the 16 variables of the 4×4 matrix are known, one can build the appropriate one-to-one relationship between the extrinsic and intrinsic Y -parameters. The next step is to measure design test structures for determining the four-port parameters. Since for each test structure one can measure a 2×2 Y -parameter matrix, one obtains four equations in each ac measurement. To solve for all 16 variables, one needs to measure at least four different test structures, unless approximations are made.

The industry-standard “open-short” deembedding method only uses two test structures: an open and a short, together with an equivalent-circuit model. Fig. 2 shows the equivalent-circuit model of this traditional “open-short” deembedding method. One can see that the distributed parasitics are simplified into one parallel capacitor (G) at the extrinsic end and two series inductors (Z) between the extrinsic and intrinsic ends. The intrinsic device Y -parameters can thus be calculated by

$$Y^{\text{INT}} = \left[(Y^{\text{DUT}} - Y^{\text{OPEN}})^{-1} - (Y^{\text{SHORT}} - Y^{\text{OPEN}})^{-1} \right]^{-1} \quad (5)$$

where $[Y^{\text{DUT}}]$, $[Y^{\text{INT}}]$, $[Y^{\text{OPEN}}]$, and $[Y^{\text{SHORT}}]$ are the Y -parameters of the DUT, intrinsic device, open structure, and short structure, respectively. Using this method on a four-port system, one gets $V_i = 0$ for the short structure and $I_i = 0$ for the open structure. Applying these two boundary conditions to (2), one obtains

$$\begin{aligned} Y^{\text{SHORT}} &= Y_{ee} \\ Y^{\text{OPEN}} &= Y_{ee} - Y_{ei}(Y_{ii})^{-1}Y_{ie}. \end{aligned}$$

Putting the above equations to (5), after simplification, yields

$$\begin{aligned} Y_X + Y_B &= Y_X Y_B^{-1} Y_{ie} Y_X^{-1} Y_{ei} + Y_X Y_B^{-1} Y_{ie} Y_B^{-1} Y_{ei} \\ Y_X &= Y^{\text{DUT}} - Y^{\text{SHORT}} \\ Y_B &= Y^{\text{SHORT}} - Y^{\text{OPEN}}. \end{aligned}$$

Without loss of generality, Y_X can be any matrix and, thus, the equalities above hold when

$$Y_{ie} = Y_{ei} = Y_{ii} = Y^{\text{SHORT}} - Y^{\text{OPEN}}. \quad (6)$$

Equation (6) gives the condition (assumption) for when the “open-short” approach is valid. At high frequencies (e.g., $f > 30$ GHz), however, this assumption is clearly no longer valid because the distributed nature of the parasitics must be considered.

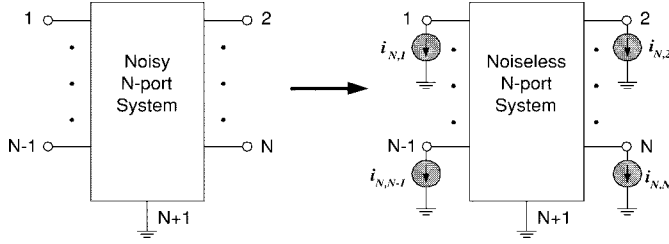


Fig. 3. Equivalent circuit of the noise current model for an n -port system. Here, $i_{n,i}$ is the equivalent noise current at port i .

B. Noise Deembedding Theory

To simplify the deembedding procedure and apply it to broadband noise extraction, we use the noise current correlation matrix SY to represent a generalized noisy system. Fig. 3 shows the equivalent circuit of the noise current model for an n -port system [11], [12]. The correlation matrix can be written as

$$SY = \begin{bmatrix} \overline{i_{n,1}i_{n,1}^*} & \cdots & \overline{i_{n,1}i_{n,n}^*} \\ \vdots & \ddots & \vdots \\ \overline{i_{n,n}i_{n,1}^*} & \cdots & \overline{i_{n,n}i_{n,n}^*} \end{bmatrix}$$

where $i_{n,j}$, $j = 1, 2, 3, \dots$ is the noise current source at port j .

In a two-port system, the minimum noise figure F_{\min} , noise impedance R_n , and optimum noise admittance Y_{opt} can be directly converted into the noise current correlation matrix SY_2 (see Appendix A).

Once we obtain the 4×4 Y -matrix, the noise deembedding method is thus straightforward [9]. Fig. 4 shows the equivalent circuit of the noise model of the DUT. For accurately modeling the four-port parasitic noise behavior, four noise current sources \vec{i}_n and the 4×4 noise current correlation matrix SY_4 are used. The noise current sources and the correlation matrix can be written as

$$\begin{aligned} SY_4 &= \begin{bmatrix} SY_{n,11} & SY_{n,12} & SY_{n,13} & SY_{n,14} \\ SY_{n,21} & SY_{n,22} & SY_{n,23} & SY_{n,24} \\ SY_{n,31} & SY_{n,32} & SY_{n,33} & SY_{n,34} \\ SY_{n,41} & SY_{n,42} & SY_{n,43} & SY_{n,44} \end{bmatrix} \\ &= \begin{bmatrix} \overline{i_{n,1}i_{n,1}^*} & \overline{i_{n,1}i_{n,2}^*} & \overline{i_{n,1}i_{n,3}^*} & \overline{i_{n,1}i_{n,4}^*} \\ \overline{i_{n,2}i_{n,1}^*} & \overline{i_{n,2}i_{n,2}^*} & \overline{i_{n,2}i_{n,3}^*} & \overline{i_{n,2}i_{n,4}^*} \\ \overline{i_{n,3}i_{n,1}^*} & \overline{i_{n,3}i_{n,2}^*} & \overline{i_{n,3}i_{n,3}^*} & \overline{i_{n,3}i_{n,4}^*} \\ \overline{i_{n,4}i_{n,1}^*} & \overline{i_{n,4}i_{n,2}^*} & \overline{i_{n,4}i_{n,3}^*} & \overline{i_{n,4}i_{n,4}^*} \end{bmatrix} \\ &= \vec{i}_n \vec{i}_n^* \end{aligned}$$

where $SY_{n,ij}$, i , and $j = 1, 2, 3, 4$ are the noise current correlation between ports i and j . For brevity, \vec{i}_n and SY_4 are also written as

$$\begin{aligned} \vec{i}_n &= \begin{pmatrix} i_{n,1} \\ i_{n,2} \\ i_{n,3} \\ i_{n,4} \end{pmatrix} = \begin{pmatrix} i_{n,e} \\ i_{n,i} \end{pmatrix} \\ SY_4 &= \begin{bmatrix} SY_{n,ee} & SY_{n,ei} \\ SY_{n,ie} & SY_{n,ii} \end{bmatrix} = 4kT \text{Real} \left(\begin{bmatrix} Y_{ee} & Y_{ei} \\ Y_{ie} & Y_{ii} \end{bmatrix} \right) \end{aligned}$$

where $i_{n,e}$ and $i_{n,i}$ are extrinsic and intrinsic noise current sources, respectively.

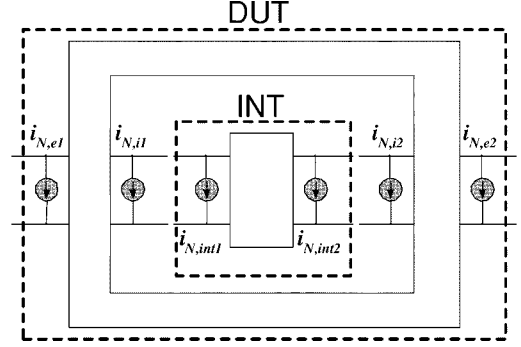


Fig. 4. Equivalent circuit of the noise model of the DUT. Here, $i_{n,e1}$, $i_{n,e2}$, $i_{n,i1}$, and $i_{n,i2}$ are noise current sources at ports 1–4, respectively, and $i_{n,int1}$ and $i_{n,int2}$ are the noise current sources of the intrinsic two-port system.

The four-port I - V relation of the DUT, considering noise currents, can then be written as

$$\begin{pmatrix} I_e + i_{n,e} \\ I_i + i_{n,i} + i_{n,int} \end{pmatrix} = \begin{bmatrix} Y_{ee} & Y_{ei} \\ Y_{ie} & Y_{ii} \end{bmatrix} \begin{pmatrix} V_e \\ V_i \end{pmatrix}. \quad (7)$$

One can thus calculate the intrinsic noise correlation matrix as (see Appendix B)

$$\begin{aligned} SY_{n,int} &= (Y_T)^{-1} (SY_{n,total} - SY_{n,ee}) (Y_T^*)^{-1} \\ &\quad - SY_{n,ii} + (Y_T)^{-1} SY_{n,ei} + SY_{n,ie} (Y_T^*)^{-1} \end{aligned} \quad (8)$$

where $Y_T = Y_{ei}(Y^{\text{INT}} + Y_{ii})^{-1}$.

III. TEST STRUCTURES AND DEEMBEDDING METHODOLOGY

To obtain the values of the 16 elements in the 4×4 matrix, a direct approach is to use more test structures to obtain more boundary conditions. Referring to (3), one obtains the matrix of $Y_{ei}(Y_{\text{test,int}} + Y_{ii})^{-1}Y_{ie}$ using $Y_{\text{test}} - Y^{\text{SHORT}}$, where Y_{test} are the measured Y -parameters and $Y_{\text{test,int}}$ are the intrinsic Y -parameters of the test structures. One can obtain various $Y_C = Y_{\text{test,int}} + Y_{ii}$ by carefully choosing different testing structures and then linearly expanding the measured matrices. In this method, we are attempting to obtain matrices in the form of

$$\begin{aligned} Y^{\text{LO}} &= Y_{ei} \begin{bmatrix} 0 & 0 \\ 0 & a \end{bmatrix} Y_{ie} \\ Y^{\text{RO}} &= Y_{ei} \begin{bmatrix} b & 0 \\ 0 & 0 \end{bmatrix} Y_{ie} \\ Y^{\text{TS}} &= Y_{ei} \begin{bmatrix} c & c \\ c & c \end{bmatrix} Y_{ie} \end{aligned}$$

where a , b , and c are constants. Thus, Y_{ei} and Y_{ie} can be calculated using

$$Y_{ie} = k_t Y'_{ei} = k_t \begin{bmatrix} 1 & \frac{y_{12}^{\text{RO}}}{y_{11}^{\text{RO}}} \\ m_1 & m_1 \frac{y_{12}^{\text{LO}}}{y_{11}^{\text{LO}}} \end{bmatrix} \quad (9)$$

$$Y_{ei} = k_r Y'_{ie} = k_r \begin{bmatrix} 1 & m_2 \\ \frac{y_{21}^{\text{RO}}}{y_{11}^{\text{RO}}} & m_2 \frac{y_{21}^{\text{LO}}}{y_{11}^{\text{LO}}} \end{bmatrix} \quad (10)$$

$$Y_{ii} = k_t k_r Y'_{ie} (Y^{\text{SHORT}} - Y^{\text{OPEN}})^{-1} Y'_{ei} \quad (11)$$

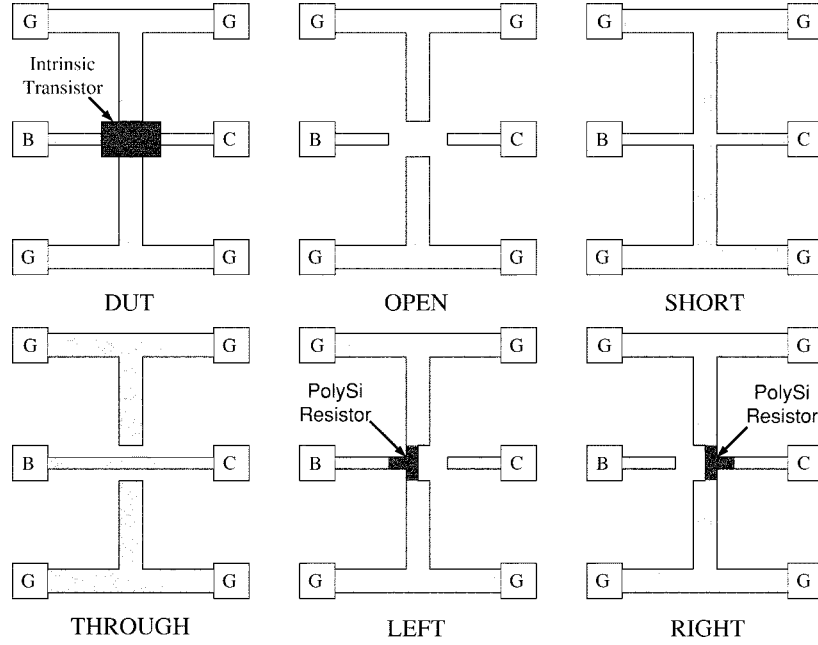


Fig. 5. Layout of the DUT and the required test structures.

$$m_1 = \frac{\frac{y_{12}^{TS}}{y_{11}^{TS}} - \frac{y_{12}^{RO}}{y_{11}^{RO}}}{\frac{y_{12}^{LO}}{y_{11}^{LO}} - \frac{y_{12}^{TS}}{y_{11}^{TS}}}$$

$$m_2 = \frac{\frac{y_{21}^{TS}}{y_{11}^{TS}} - \frac{y_{21}^{RO}}{y_{11}^{RO}}}{\frac{y_{21}^{LO}}{y_{11}^{LO}} - \frac{y_{21}^{TS}}{y_{11}^{TS}}}$$

where k_l and k_r are scale factors and will be determined below.

To obtain the matrices discussed above, five test structures are needed. Fig. 5 shows the layout of the DUT and the required test structures. The $Y_{\text{test,int}} + Y_{ii}$ for OPEN, LEFT, RIGHT, and THROUGH test structures are

$$Y_{\text{open,int}} + Y_{ii} = \begin{bmatrix} Y_{ii,11} & Y_{ii,12} \\ Y_{ii,21} & Y_{ii,22} \end{bmatrix} \quad (12)$$

$$Y_{\text{left,int}} + Y_{ii} = \begin{bmatrix} Y_{ii,11} + g_l & Y_{ii,12} \\ Y_{ii,21} & Y_{ii,22} \end{bmatrix} \quad (13)$$

$$Y_{\text{right,int}} + Y_{ii} = \begin{bmatrix} Y_{ii,11} & Y_{ii,12} \\ Y_{ii,21} & Y_{ii,22} + g_r \end{bmatrix} \quad (14)$$

$$Y_{\text{through,int}} + Y_{ii} = \begin{bmatrix} Y_{ii,11} + A & Y_{ii,12} - A \\ Y_{ii,21} - A & Y_{ii,22} + A \end{bmatrix} \quad (15)$$

$A \rightarrow \infty$

where $g_l = 1/R_l$ and $g_r = 1/R_r$ are conductances of the resistors in the LEFT and RIGHT structures, respectively.

One can prove (see Appendix C) that

$$Y^{\text{LEFT}} - xY^{\text{OPEN}} - (1-x)Y^{\text{SHORT}} = Y_{ei} \begin{bmatrix} 0 & 0 \\ 0 & a \end{bmatrix} Y_{ie}$$

$$Y^{\text{RIGHT}} - yY^{\text{OPEN}} - (1-y)Y^{\text{SHORT}} = Y_{ei} \begin{bmatrix} b & 0 \\ 0 & 0 \end{bmatrix} Y_{ie}$$

$$Y^{\text{THRU}} - zY^{\text{OPEN}} - (1-z)Y^{\text{SHORT}} = Y_{ei} \begin{bmatrix} c & c \\ c & c \end{bmatrix} Y_{ie}$$

by solving for x , y , and z in the following:

$$|Y^{\text{LEFT}} - xY^{\text{OPEN}} - (1-x)Y^{\text{SHORT}}| = 0 \quad (16)$$

$$|Y^{\text{RIGHT}} - yY^{\text{OPEN}} - (1-y)Y^{\text{SHORT}}| = 0 \quad (17)$$

$$|Y^{\text{THRU}} - zY^{\text{OPEN}} - (1-z)Y^{\text{SHORT}}| = 0 \quad (18)$$

and choosing the solution $x \neq 1$, $y \neq 1$, and $z \neq 1$. Taking (9)–(11) into (4), one gets

$$Y^{\text{INT}} = -k_r k_l Y'_{ie} (Y^{\text{DUT}} - Y_{ee})^{-1} Y'_{ei} - Y'_{ii}.$$

Substituting for Y^{DUT} using Y^{LEFT} , one gets

$$\begin{aligned} Y^{\text{left,int}} &= -k_r k_l \left(Y'_{ie} (Y^{\text{DUT}} - Y_{ee})^{-1} Y'_{ei} - Y'_{ii} \right) \\ &= k_r k_l Y^{\text{LINT}} \\ &= \begin{bmatrix} g_l & 0 \\ 0 & 0 \end{bmatrix} \end{aligned} \quad (19)$$

where $Y^{\text{LINT}} = -Y'_{ie} (Y^{\text{DUT}} - Y_{ee})^{-1} Y'_{ei} - Y'_{ii}$. Thus $k_r k_l = g_l / Y_{11}^{\text{LINT}}$.

Finding the product of k_r and k_l is sufficient to deembed the Y -parameters, but is not sufficient in order to deembed the noise correlation matrix. Rather, one needs to obtain the value of k_r and k_l , respectively. To determine these values, one must use the general nature of the passive system

$$4kT \text{Real}(Y_{ij}) = \overline{i_{n,i} i_{n,j}^*} = (\overline{i_{n,j} i_{n,i}^*})^* = 4kT \text{Real}(Y_{ji}).$$

$\text{Real}(Y_{ei,11}) = \text{Real}(Y_{ie,11})$ and, hence, $k_r = k_l = \sqrt{g_l / Y_{11}^{\text{LINT}}}$.

At this point, all 16 elements of the 4×4 matrix are determined. The intrinsic Y -parameters and broad-band noise characteristics can thus be obtained using (4) and (8).

IV. NONIDEALITIES AND VALIDITY CHECK

In reality, test structures can never be perfectly ideal. It is thus necessary to check the validity of the proposed deembedding methodology using nonideal test structures. The assumptions made in this method are that (12)–(15) and $Y_{ee} + Y_{ei}(Y_{\text{short,int}} + Y_{ii})^{-1}Y_{ie} \approx Y_{ee}$ hold. Since one solution of x , y , and z should be one, one can check the validity of the first four equations by solving x , y , and z from the measured data. One cannot check the validity of the last equation, however, by simply manipulating the measured data.

In the current SiGe HBT technology, the intrinsic device layout size is smaller than a few tens of micrometers, although the DUT size (including pads, etc.) is several hundreds of micrometers and, thus, the assumptions are valid in the millimeter-wave band with optimized layout design. In higher frequency measurements (i.e., $f > 300$ GHz), if one can accurately estimate the nonideal intrinsic S -parameters of the test structures, the methodology will remain useful with a few modifications in the extraction equations.

V. SUMMARY OF THE PROPOSED DEEMBEDDING PROCEDURE

- 1) Measure the S -parameters of $[S^{\text{DUT}}]$, $[S^{\text{OPEN}}]$, $[S^{\text{SHORT}}]$, $[S^{\text{THRU}}]$, $[S^{\text{LEFT}}]$, and $[S^{\text{RIGHT}}]$. Convert the S -parameters into Y -parameters.
- 2) Solve for x , y , and z in the following:

$$\begin{aligned} |Y^{\text{LEFT}} - xY^{\text{OPEN}} - (1-x)Y^{\text{SHORT}}| &= 0 \\ |Y^{\text{RIGHT}} - yY^{\text{OPEN}} - (1-y)Y^{\text{SHORT}}| &= 0 \\ |Y^{\text{THRU}} - zY^{\text{OPEN}} - (1-z)Y^{\text{SHORT}}| &= 0. \end{aligned}$$

Choose the solution $x \neq 1$, $y \neq 1$, and $z \neq 1$.

- 3) Let

$$\begin{aligned} Y^{\text{LO}} &= Y^{\text{LEFT}} - xY^{\text{OPEN}} - (1-x)Y^{\text{SHORT}} \\ Y^{\text{RO}} &= Y^{\text{RIGHT}} - yY^{\text{OPEN}} - (1-y)Y^{\text{SHORT}} \\ Y^{\text{TS}} &= Y^{\text{THRU}} - zY^{\text{OPEN}} - (1-z)Y^{\text{SHORT}} \end{aligned}$$

and obtain unscaled $[Y'_{ei}]$, $[Y'_{ie}]$, and $[Y'_{ii}]$ by using (9)–(11).

- 4) Calculate the scale factor k using (19).
- 5) Calculate the intrinsic Y -parameters using (4).
- 6) Calculate the intrinsic noise correlation matrix using (8).

VI. MEASUREMENT AND VERIFICATION

To compare the various deembedding methods, the S -parameters of state-of-the-art $0.12 \times 2.5 \mu\text{m}^2$ SiGe HBTs were measured (Fig. 6).

The peak f_T of these SiGe HBTs is 180 GHz for a $BV_{\text{CEO}} = 2.2$ V. The measurements were performed using a conventional microwave probing system and an HP 8510C vector network analyzer over a frequency range of 4–36 GHz.

Fig. 7 compares the measured and “open-short” deembedded S -parameters. Note that, for a better comparison, we have plotted $S_{21}/4$ and $S_{22} - 1$ instead of S_{21} and S_{22} . Observe

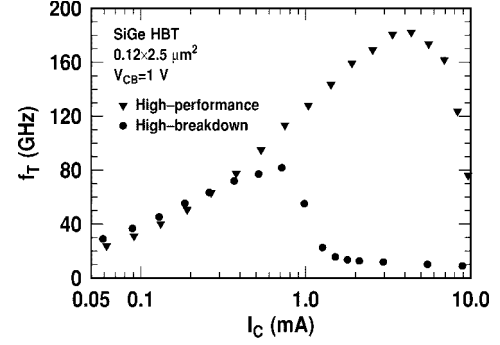


Fig. 6. Measured cutoff frequency characteristics of the state-of-the-art SiGe HBTs used for verification.

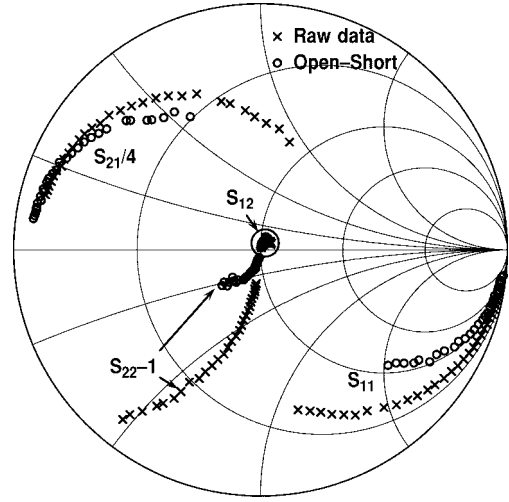


Fig. 7. Measured and deembedded S -parameters. The device was biased at $I_C = 2$ mA and $V_{CB} = 1$ V.

that a large deviation is seen between the raw and deembedded data. This is because the parasitics are comparable to the intrinsic device Y -parameters in these small-sized devices. A more sophisticated deembedding method is clearly required for accurate characterization of such high-speed devices.

To fully verify the accuracy of the proposed new four-port deembedding methodology at high frequencies, and to make a fair comparison with other deembedding techniques, one must resort to device simulations because the (implicitly accurate) simulated intrinsic device S -parameters are needed to quantify accuracy of the various deembedding methods.

Several equivalent circuits were chosen to determine how a given parasitic model impacts the various deembedding methods. Fig. 8 shows three equivalent circuits of the parasitics. The component values in each circuit were extracted and optimized from the measured S -parameters of parasitics. A device model carefully calibrated to measured data was used in HP-ADS to simulate the S -parameters of the SiGe HBTs both with and without the parasitics. The simulated frequency range was 1–100 GHz. Fig. 9 shows the deembedded Y -parameters after applying both the “open-short” and the new four-port method on each parasitic model.

For equivalent-circuit model 1, the intrinsic Y -parameters are accurately deembedded using both the four-port and

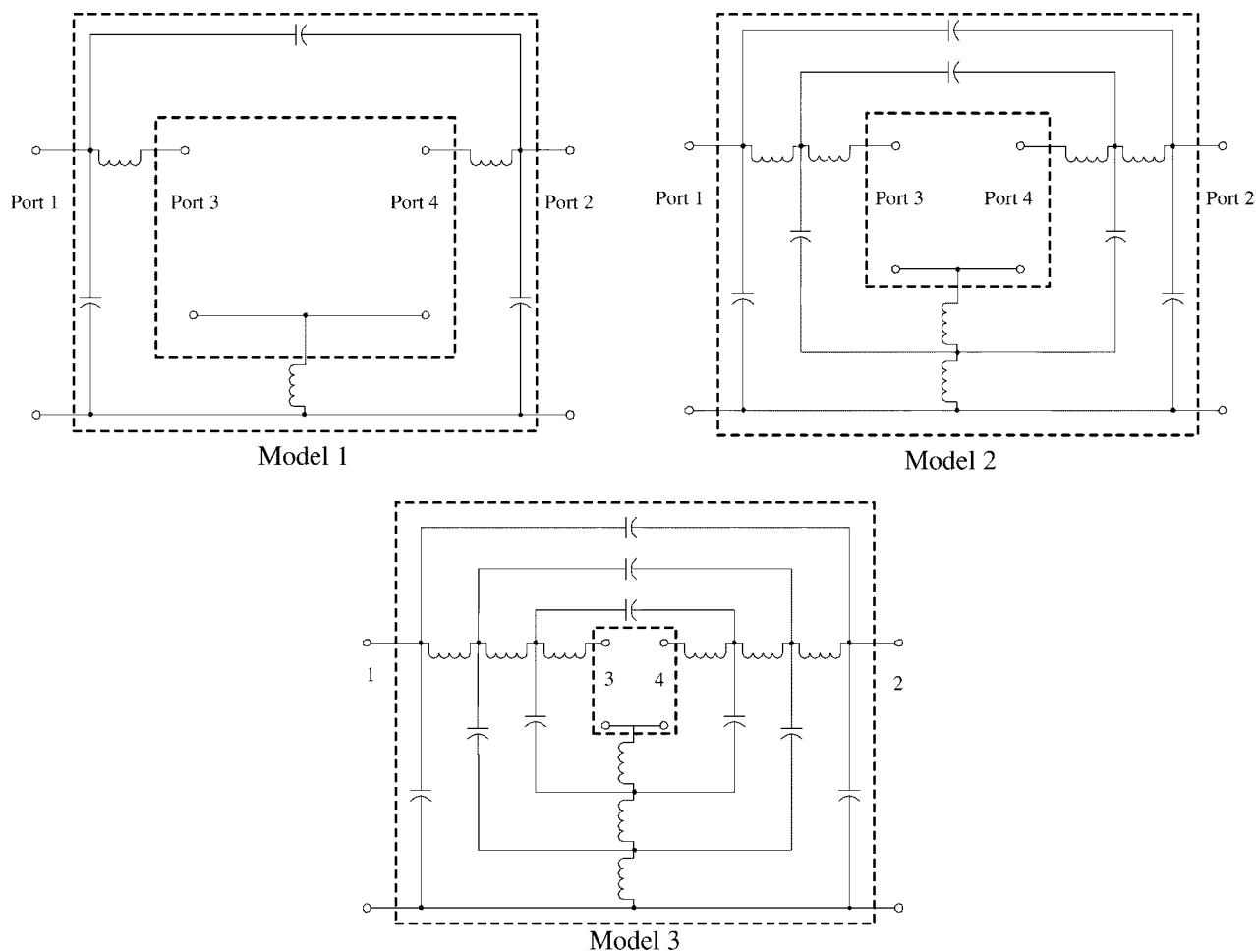


Fig. 8. Three equivalent-circuit models of the parasitics used in the simulations.

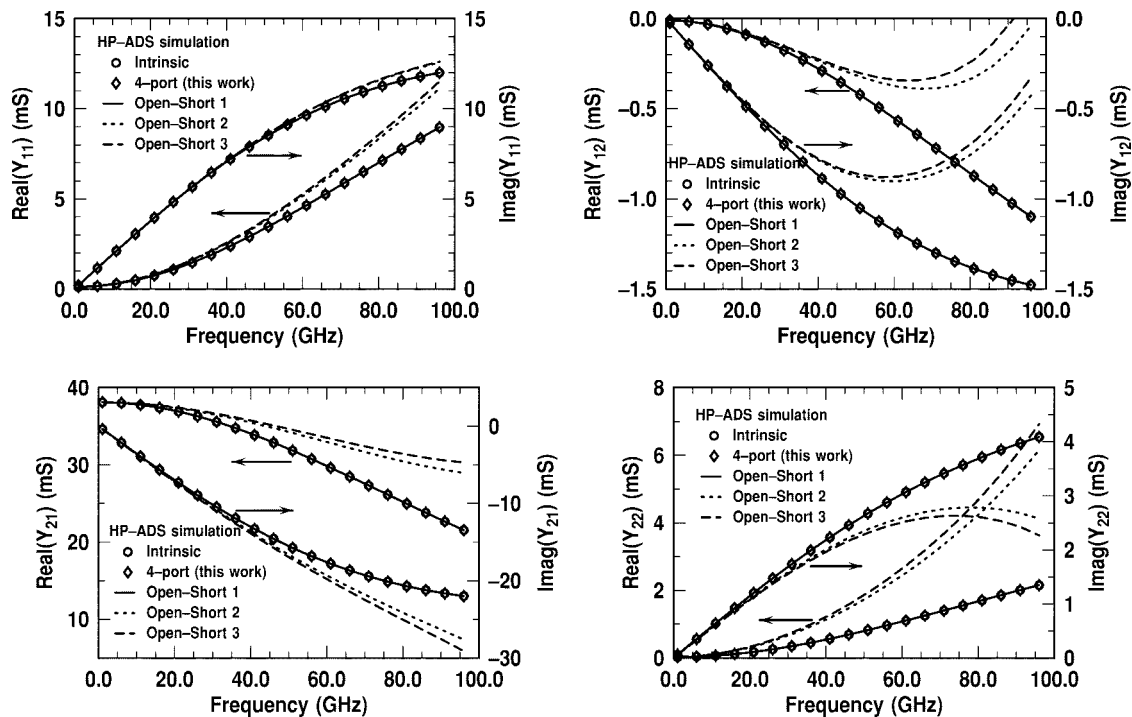


Fig. 9. Real and imaginary parts of the intrinsic and deembedded Y -parameters obtained using both the new four-port and traditional "open-short" technique on each of the three equivalent-circuit models.

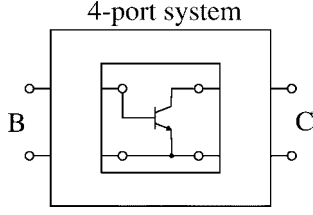
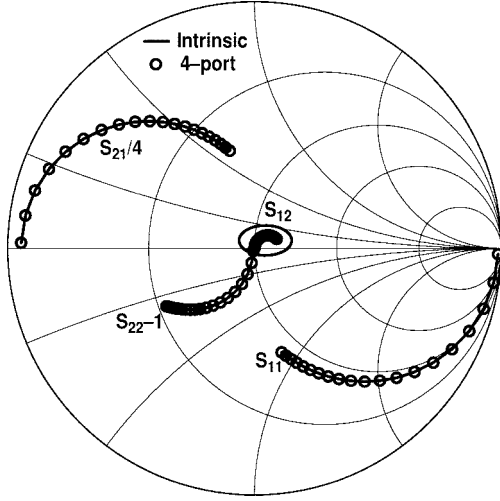


Fig. 10. Equivalent circuit of the DUT used in the HP-ADS simulations.

Fig. 11. Simulated intrinsic and four-port deembedded S -parameters. The frequency range is from 1 to 100 GHz.

“open–short” method. For equivalent-circuit models 2 and 3, however, observe that the “open–short” method produces large deviations from the intrinsic Y -parameters at frequencies above approximately 30 GHz. This clearly demonstrates the potential inaccuracy of the traditional “open–short” method at high frequencies. Observe as well that the accuracy of the new four-port method is not dependent on the choice of the equivalent circuit or the frequency.

Without loss of generality, we can arbitrarily choose the four-port Y -parameters as a parasitic system in Fig. 10 and then extract the Y -parameters using the proposed four-port method. Fig. 11 shows the simulated intrinsic and four-port deembedded S -parameters. Excellent agreement is observed across the entire frequency range. In general, the current method is valid for any four-port parasitic system and, thus, should also be suitable for package deembedding, where wire-bonds, for instance, must be carefully considered.

The noise characteristics were also simulated and compared in HP-ADS on the same device. Fig. 12 shows the noise characteristics of DUT, both intrinsic and deembedded, using both the traditional “open–short” and the new four-port method. The results again show good precision using the four-port method. For the “open–short” technique, NF_{\min} and Γ_{opt} are deembedded correctly for a wider frequency range (up to 60 GHz). Note, however, that R_n is underestimated at frequencies above approximately 30 GHz. Hence for an accurate noise characterization of SiGe HBTs at high frequencies, the new four-port deembedding methodology is also preferred.

VII. SUMMARY

We have proposed a new four-port S -parameter and broadband noise deembedding methodology that is useful for high-frequency characterization transistors. The method requires no equivalent-circuit modeling or detailed EM simulations. Systematic four-port analysis and mathematical derivations are presented to prove the validity of the method. Detailed comparisons between the traditional “open–short” method and this new four-port method were performed using measurements and calibrated simulations of state-of-the-art SiGe HBTs. The results clearly demonstrate that this method is more accurate than the industry-standard “open–short” method. Based on HP-ADS simulations using calibrated SiGe HBT models, one can correctly extract S -parameters and noise characteristics at least to 100 GHz, and this new four-port method should also prove useful for extracting package parasitics in complex systems.

APPENDIX

A. TWO-PORT NOISE CHARACTERISTICS AND CORRELATION MATRIX

The minimum noise figure F_{\min} , noise impedance R_n , optimum noise admittance Y_{opt} , and noise current correlation SY_2 can be related by [13]

$$\begin{aligned} c_{A,11} &= 4kTR_n \\ c_{A,12} &= 4kT \left(\frac{F_{\min} - 1}{2} - R_n Y_{\text{opt}}^* \right) \\ c_{A,21} &= C_{A,12}^* \\ c_{A,22} &= 4kTR_n |Y_{\text{opt}}|^2 \\ SY_2 &= AC_A A^* \end{aligned}$$

where

$$\begin{aligned} A &= \begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix} \\ C_A &= \begin{bmatrix} c_{A,11} & c_{A,12} \\ c_{A,21} & c_{A,22} \end{bmatrix}. \end{aligned}$$

B. FOUR-PORT NOISE CORRELATION MATRIX DEEMBEDDING

Substituting $I_i = -Y^{\text{INT}} V_i$ into (7), one obtains

$$\begin{aligned} I_e + i_{n,e} - Y_{ei}(Y^{\text{INT}} + Y_{ii})^{-1}(i_{n,i} + i_{n,\text{int}}) \\ = [Y_{ee} - Y_{ei}(Y^{\text{INT}} + Y_{ii})^{-1}Y_{ie}] V_e \\ \Rightarrow i_{n,\text{total}} \\ = i_{n,e} - Y_{ei}(Y^{\text{INT}} + Y_{ii})^{-1}(i_{n,i} + i_{n,\text{int}}) \end{aligned}$$

where $i_{n,\text{total}}$ are the equivalent noise current sources at the extrinsic ports. The resultant noise correlation is shown in the equation at the bottom of the following page.

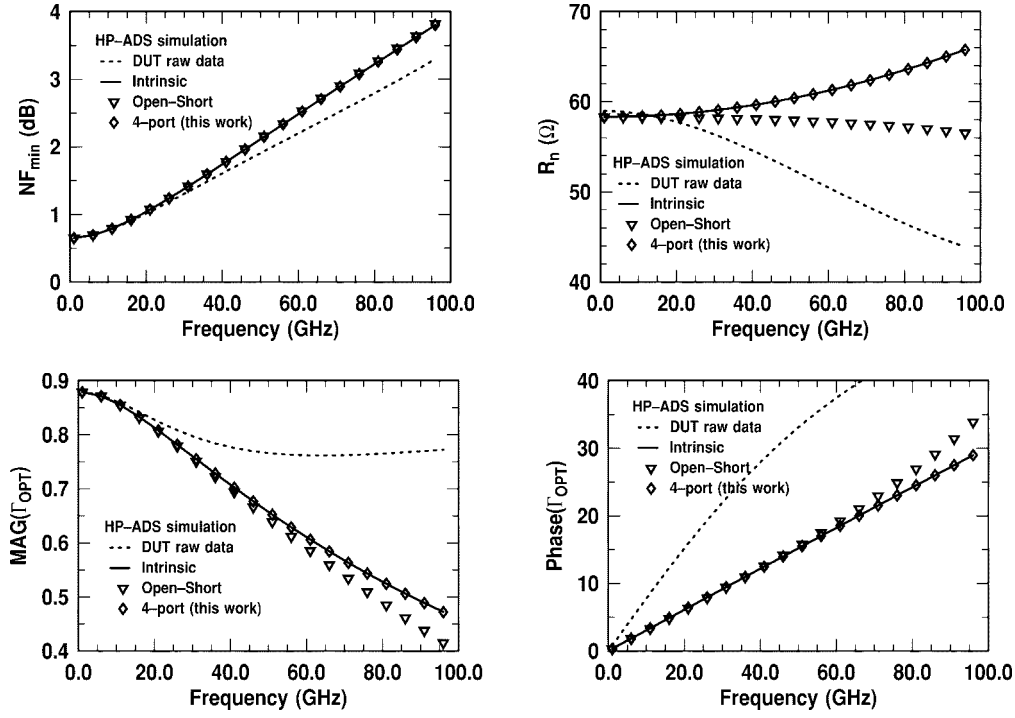


Fig. 12. Noise characteristics of the DUT, both intrinsic and deembedded using the “open-short” method and the proposed four-port method.

Note that the intrinsic device noise sources and parasitic noise sources are uncorrelated and, thus, one obtains

$$\begin{aligned}
 SY_{n,total} &= \overline{i_{n,e} i_{n,e}^*} + Y_{ei} (Y^{INT} + Y_{ii})^{-1} \\
 &\quad \times \left(\overline{i_{n,i} i_{n,i}^*} + \overline{i_{n,int} i_{n,int}^*} \right) \left[(Y^{INT} + Y_{ii})^{-1} \right]^* Y_{ei}^* \\
 &\quad - Y_{ei} (Y^{INT} + Y_{ii})^{-1} \overline{i_{n,i} i_{n,e}^*} - \overline{i_{n,i}^* i_{n,e}} \\
 &\quad \times \left[(Y^{INT} + Y_{ii})^{-1} \right]^* Y_{ei}^* \\
 &= SY_{n,ee} + Y_T SY_{n,ii} Y_T^* + Y_T SY_{n,int} Y_T^* \\
 &\quad - Y_T SY_{n,ie} - SY_{n,ei} Y_T^*.
 \end{aligned}$$

where

$$\begin{aligned}
 Y_T &= Y_{ei} (Y^{INT} + Y_{ii})^{-1} \\
 Y_{n,ee} &= 4kT \text{Real}(Y_{ee}) \\
 Y_{n,ei} &= 4kT \text{Real}(Y_{ei}) \\
 Y_{n,ie} &= 4kT \text{Real}(Y_{ie}) \\
 Y_{n,ii} &= 4kT \text{Real}(Y_{ii}).
 \end{aligned}$$

Hence, the intrinsic noise current correlation matrix can be calculated as

$$\begin{aligned}
 SY_{n,int} &= (Y_T)^{-1} (SY_{n,total} - SY_{n,ee}) (Y_T^*)^{-1} \\
 &\quad - SY_{n,ii} + (Y_T)^{-1} SY_{n,ei} + SY_{n,ie} (Y_T^*)^{-1}. \quad (20)
 \end{aligned}$$

C. LINEAR EXPANSION OF THE Y -PARAMETERS OF THE TEST STRUCTURES

The $Y_{test,int} + Y_{ii}$ for the OPEN, LEFT, RIGHT, and THROUGH test structures are

$$\begin{aligned}
 Y_{open,int} + Y_{ii} &= \begin{bmatrix} Y_{ii,11} & Y_{ii,12} \\ Y_{ii,21} & Y_{ii,22} \end{bmatrix} \\
 Y_{left,int} + Y_{ii} &= \begin{bmatrix} Y_{ii,11} + g_l & Y_{ii,12} \\ Y_{ii,21} & Y_{ii,22} \end{bmatrix} \\
 Y_{right,int} + Y_{ii} &= \begin{bmatrix} Y_{ii,11} & Y_{ii,12} \\ Y_{ii,21} & Y_{ii,22} + g_r \end{bmatrix} \\
 Y_{through,int} + Y_{ii} &= \begin{bmatrix} Y_{ii,11} + A & Y_{ii,12} - A \\ Y_{ii,21} - A & Y_{ii,22} + A \end{bmatrix}.
 \end{aligned}$$

Consider $(Y_{open,int} + Y_{ii})^{-1}$ and $(Y_{left,int} + Y_{ii})^{-1}$ as follows:

$$\begin{aligned}
 (Y_{open,int} + Y_{ii})^{-1} &= \begin{bmatrix} \frac{Y_{ii,22}}{D} & \frac{-Y_{ii,12}}{D} \\ \frac{-Y_{ii,21}}{D} & \frac{Y_{ii,11}}{D} \end{bmatrix} \\
 (Y_{left,int} + Y_{ii})^{-1} &= \begin{bmatrix} \frac{Y_{ii,22}}{(D + g_l Y_{ii,22})} & \frac{-Y_{ii,12}}{(D + g_l Y_{ii,22})} \\ \frac{-Y_{ii,21}}{(D + g_l Y_{ii,22})} & \frac{(Y_{ii,11} + g_l)}{(D + g_l Y_{ii,22})} \end{bmatrix}
 \end{aligned}$$

$$SY_{n,total} = \overline{i_{n,total} \times i_{n,total}^*} = \left[i_{n,e} - Y_{ei} (Y^{INT} + Y_{ii})^{-1} (i_{n,i} + i_{n,int}) \right] \times \left[i_{n,e} - Y_{ei} (Y^{INT} + Y_{ii})^{-1} (i_{n,i} + i_{n,int}) \right]^*$$

$$\begin{vmatrix} Y_{ii,22} \left[\frac{1}{(D + gY_{ii,22})} - \frac{1}{D} \right] & -Y_{ii,12} \left[\frac{1}{(D + gY_{ii,22})} - \frac{1}{D} \right] \\ -Y_{ii,21} \left[\frac{1}{(D + gY_{ii,22})} - \frac{1}{D} \right] & Y_{ii,11} \left[\frac{1}{(D + gY_{ii,22})} - \frac{1}{D} \right] + \frac{g}{(D + gY_{ii,22})} \end{vmatrix} = 0 \Rightarrow |Y^{\text{LEFT}} - Y^{\text{OPEN}}| = 0$$

where $D = |Y_{ii}| = Y_{ii,11}Y_{ii,22} - Y_{ii,12}Y_{ii,21}$. If we choose $x = D/(D + gY_{ii,22})$, then

$$\begin{aligned} Y^{\text{LEFT}} - xY^{\text{OPEN}} - (1-x)Y^{\text{SHORT}} \\ = Y_{ei} [(Y_{\text{left,int}} + Y_{ii})^{-1} - x(Y_{\text{open,int}} + Y_{ii})^{-1}] Y_{ie} \\ = Y_{ei} \begin{bmatrix} 0 & 0 \\ 0 & a \end{bmatrix} Y_{ie} \end{aligned}$$

where $a = g/(D + gY_{ii,22})$. Thus, $x = D/(D + gY_{ii,22})$ is one solution of $Y^{\text{LEFT}} - xY^{\text{OPEN}} - (1-x)Y^{\text{SHORT}} = 0$.

On the other hand, see the equation shown at the top of this page.

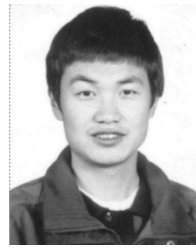
Hence, $D/(D + gY_{ii,22})$ and 1 are the only two solutions of (16). Similarly one can prove $D/(D + gY_{ii,11})$ and 1 are the only two solutions of (17); $D/(D + A(Y_{ii,11} + Y_{ii,12} + Y_{ii,21} + Y_{ii,22}))$ and 1 are the only two solutions of (18). Thus, the values of x , y , and z are fully determined.

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REFERENCES

- [1] P. J. van Wijn *et al.*, "A new straightforward calibration and correction procedure for "on wafer" high-frequency S -parameter measurements (45 MHz–18 GHz)," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Sept. 1987, pp. 70–73.
- [2] A. Fraser *et al.*, "GHz on-silicon-wafer probing calibration methods," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Sept. 1988, pp. 154–157.
- [3] M. C. A. M. Koolen *et al.*, "An improved de-embedding technique for on-wafer high-frequency characterization," in *Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Sept. 1991, pp. 188–191.
- [4] H. Cho *et al.*, "A three-step method for the de-embedding of high-frequency S -parameter measurements," *IEEE Trans. Electron Devices*, vol. 38, pp. 1371–1375, June 1991.
- [5] E. P. Vandamme *et al.*, "Improved three-step de-embedding method to accurately account for the influence of pad parasitics in silicon on-wafer RF test-structures," *IEEE Trans. Electron Devices*, vol. 48, pp. 737–742, Apr. 2001.
- [6] C. H. Chen *et al.*, "A general noise and S -parameter deembedding procedure for on-wafer high-frequency noise measurements of MOSFETs," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 1004–1005, May 2001.
- [7] R. Mahmoudi *et al.*, "A five-port de-embedding method for floating two-port networks," *IEEE Trans. Instrum. Meas.*, vol. 47, pp. 482–488, Apr. 1998.
- [8] V. Rizzoli *et al.*, "Computer-aided noise analysis of MESFET and HEMT mixers," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1401–1410, Sept. 1989.
- [9] R. A. Pucel *et al.*, "A general noise de-embedding procedure for packaged two-port linear active devices," *IEEE Trans. Microwave Theory Tech.*, vol. 40, pp. 2013–2024, Nov. 1992.
- [10] S. Bousnina *et al.*, "An accurate on-wafer deembedding technique with application to HBT device characterization," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 420–424, Feb. 2002.
- [11] H. Hillbrand *et al.*, "Rauschanalyse von linearen netzwerken," *Wiss. Ber. AEG-Telefunken*, vol. 49, pp. 127–138, 1976.
- [12] F. Bonani *et al.*, "An efficient approach to noise analysis through multi-dimensional physics-based models," *IEEE Trans. Electron Devices*, vol. 45, pp. 261–269, Jan. 1998.
- [13] H. Hillbrand *et al.*, "An efficient method for computer aided noise analysis of linear amplifier networks," *IEEE Trans. Circuits Syst.*, vol. CAS-23, pp. 235–238, Apr. 1976.



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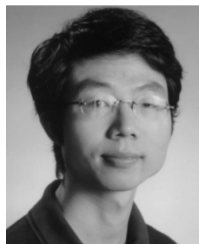


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